RF AMPLIFIER WITH CURRENT MIRROR BIAS-BOOSTING

TECHNICAL FIELD

The present invention relates to power amplifiers, and more specifically, to an improved bias boosting technique for power amplifiers suitable for use in high frequency applications.

BACKGROUND OF THE INVENTION

A linear RF power amplifier is commonly biased in class AB operation so as to achieve higher power-added efficiency. Such an amplifier is commonly used in the output stage of high-frequency power amplifiers. However, in a conventionally biased class AB amplifier, the average bias supply current increases as RF input power increases. This increased average current results in an increased voltage drop in the resistive part of the bias circuit. This in turn reduces the average voltage drop across the forward-biased PN junction of the power amplifying transistor, pushing the amplifier into class B and even class C operations. Therefore, the output power will be saturated as the input power further increases.

Class AB amplifiers are commonly used in high-frequency amplifiers. Linear RF amplifiers are usually biased in a class AB operation to achieve higher power-added efficiency ("PAE").

In a conventionally biased class AB amplifier, as radio frequency ("RF") input power increases, the average bias supply-current increases. This increased average direct current ("DC") results in an increased voltage drop in the resistive part of the bias circuit. This increased voltage drop across the biasing resistor, in turn, reduces the voltage drop

across the forward-biased PN junction of the amplifying transistor, thereby saturating its large signal transconductance and reducing its gain. Thus, as RF input power increases, the amplifier may be pushed into class B operations (in which conduction takes place during 50% of the signal cycle) or class C operations (conduction takes place during less than 50% of the signal cycle). As input power further increases, output power saturation will occur.

Boosting of the DC bias of the amplifying transistor is necessary to compensate for the aforementioned DC drop. This DC bias increase will improve linearity at higher output power levels where the class AB amplifier is in saturation or close to saturation levels, as described above. Existing techniques for providing such bias boosting have utilized two approaches. One such technique involves using a capacitor together with a biasing circuit consisting of two or more transistors. Another such technique involves using an additional RF sensing amplifier. These techniques are the subject of other recent inventions commonly owned with this patent application, and thus do not constitute prior art.

In the former technique, the bias boosting relies on the value of the capacitor. If an on-chip capacitor is used, it is relatively difficult to control its capacitance value. If an off-chip capacitor is used, it increases the number of off-chip components, thereby requiring additional valuable space, or "real estate", on the printed circuit board ("PCB").

In the latter technique, the additional RF sensing amplifier may increase the chip area of the circuit.

In view of the above, there exists a need in the art for an improved power amplifier configuration which increases the amplifier's gain, PAE and linearity, yet does

not significantly increase the chip area of the amplifier circuit or the number of off-chip components.

It is therefore an object of the present invention to provide an amplifier circuit that boosts the bias of the output stage without significantly increasing the chip area of the circuit or of the PCB comprising the circuit.

It is a further object of the present invention to provide a power amplifier circuit that permits biasing with a lower quiescent current without having a saturation effect at higher output power levels.

SUMMARY OF THE INVENTION

An amplifier circuit comprises an input stage and an output stage. The input stage is biased by means of a circuit, such as a current mirror, that senses the input signal level. As the input signal increases the average current of the sensing circuit also increases. This current is fed forward to the output stage biasing circuit to boost its bias.

The bias boosting is thus proportional to the input signal. One of the advantages of the bias scheme presented is that it allows amplifiers to be biased with a lower quiescent current without being pushed into saturation at higher output power levels.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be more clearly understood with reference to the following description, to be read in conjunction with the accompanying drawings:

Figure 1 depicts an RF power amplifier according to the method of the present invention;

Figure 1A is a simplified version of a portion of the circuit of Figure 1, highlighting the novel components;

Figure 2 depicts an RF power amplifier according to the conventional biasing scheme; and

Figure 3 depicts an existing bias circuit technique using two current sources.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 shows an exemplary RF power amplifier configuration, incorporating the novel bias boosting scheme of the present invention. As a comparison, Figure 2 depicts a schematic of a conventional RF power amplifier, without the added bias boosting scheme. These two circuits are almost identical, with the exception of the additional current mirror circuit consisting of transistors Q11 150 and Q12 151, at the top left of the figure, in Figure 1.

In these circuits, transistors Q1 152 and Q8 153 have been matched to form a current mirror circuit. Q2 155 through Q7 156 form a biasing circuit for the output stage, which is transistor Q0 160. The biasing circuit technique is shown generally at Figure 3. Such biasing technique is the subject of another recent invention commonly owned with this patent application and thus does not constitute prior art.

For ease of description Figure 1A will be used to describe the method of the present invention in detail. Figure 1A is a simplified version of the portion of the circuit of Figure 1 critical to the present invention. Figure 1A depicts the novel current mirror, the input stage biasing circuit, and the output stage. The output stage biasing circuit,

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which comprises transistors Q2 155 through Q7 156 in Figure 1, is simplified in Figure 1A to a circuit block 1A05.

When Q1 1A04 is biased in a class AB operation, its average collector current iQ1 1A50 will increase as the RF input signal level 1A51 increases, which is a typical characteristic for class AB or class B amplifiers. Since Q1 1A04 and Q8 1A03 form a current mirror circuit, the current in Q1 1A04 is mirrored in Q8 1A03. Because the identical current flows in Q8 as in Q11 1A01, as they are connected in series, this current is mirrored by the current mirror circuit consisting of transistors Q11 1A01 and Q12 1A02 into Q12 as iQ12 1A52, and thus is fed to the output stage bias circuit 1A05, entering through port 3, 1A80. The biasing circuit controls the quiescent current in Q0 1A10. With reference to Figure 1, iQ12 170 is fed into Q6 157. Consequently, the current in Q6 provides a bias boost for Q0, the amplifying transistor.

Therefore, the addition of the current mirror of Q11 and Q12 permits an added bias boost for Q0. In a linear RF amplifier whose input stage biased in a class AB mode, this configuration increases the output stage biasing level in proportion to higher input signal levels; thereby improving linearity (reduced gain compression) at higher output power levels. Inasmuch as the method of the present invention increases the bias boost proportionally to the input RF signal level, it is in fact, an adaptive bias-boosting scheme.

The placing of the current mirror is flexible vis-a-vis that of R4 290 (with respect to Fig. 2). R4 operates to control the DC current through Q8 253, and is thus a type of biasing resistor. The current mirror of the present invention may be placed below biasing resistor R4 (190 in Fig. 1 and 1A90 in Fig. 1A), as depicted in the example circuits of Figs. 1 and 1A, or above it, with R4 in series between transistors Q11 150, 1A50 and Q8

153, 1A53 (this latter possible placement of R4 is not shown in the figures). This flexibility allows the choice of the most advantageous placing as will depend upon the particular design considerations of a given circuit embodying the method of the present invention.

Simulation results indicate that the bias boosting scheme of the present invention provides benefits to the amplifier in terms of gain, PAE and linearity due to reduced gain compression. Additionally, it allows RF amplifiers to be biased with a lower quiescent current, without pushing it into saturation at higher output power levels.

In another embodiment, if further boosting is needed, a self-bias boost scheme can be used in combination with the current mirror technique of the present invention. An example of just such a self bias boost scheme, is one that which utilizes a capacitor together with a bias circuit, as discussed above.

It is anticipated by the invention that the input as well as output biasing circuits may comprise other types of current mirror circuits, in addition to the circuit described above, or other means of generating a reference current in one part of a circuit and generating proportional currents at other locations in the circuit. Further contemplated by the invention are any means which adaptively boost an amplification circuit or subcircuit by sensing an input signal and boosting the output stage bias in proportion to such input signal.

It is understood that while the foregoing describes the preferred embodiments of the invention, various other modifications and additions will be apparent to those of skill in the art. For example, this bias boosting scheme should not be limited to circuits using bipolar junction transistors ("BJTs"), as described in the above preferred embodiment.

Circuits using other amplification devices such as field effect transistors ("FETs") or derivatives of BJTs or FETS, such as the metal oxide semiconductor field effect transistor ("MOSFET"), may also fall within the scope of the present invention. The invention also covers circuits using both FETs and BJTs, or other amplifier configurations as are known, or may be known in the future, in the art. In addition, alterations to the circuit configuration may be made to suit particular design requirements.